

RESPONSE UNDER 37 C.F.R. § 1.111
U. S. Application No. 09/472,869

REMARKS

Claims 1-9 and 11 are all the claims pending in the application.

In reply to the Response filed August 12, 2003, the Examiner removed the previous claim rejection. Now, the status of the claims is the following.

Claims 1-4 are allowed.

Claims 6-9 are objected to as being dependent from a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 5 and 11 are rejected under 35 U.S.C. § 103(a) as being unpatentable over newly-cited Sokawa et al. (US 6,353,460, hereinafter "Sokawa").

Applicant submits that Sokawa fails to teach or suggest all of the limitations of claim 5. In particular, Sokawa does not disclose the format converter as claimed. Claim 5 recites a format converter for receiving either of first and second input digital signals, according to which of the first and second input digital signals is present. The format conversion section of Sokawa includes a selection circuit 1030, which selects one of the video signals output from the video signal sources 1210a to 1210d. See FIG. 1 and col. 12, lines 15-18. The selection circuit 1030 selects one of the video signals in accordance with a control signal output from a CPU 1020. See col. 12, lines 24-26. The value of the control signal is determined in accordance with user operation information input via a control input terminal 1021, and the user operation information includes a channel selection signal. Col. 13, lines 23-26. Thus, the format conversion section of Sokawa selects one of the video signals as an input, based on the channel selection of a user. By

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contrast, the format converter of claim 5 receives either the first or the second input digital signal, according to which of the first and second input digital signals is present. Therefore, claim 5 is allowable over the prior art, for at least this reason.

Also, Applicant submits that Sokawa does not teach or suggest a controller for detecting a frame rate of the input digital signal received by the format converter and outputting a timing control signal corresponding to the frame rate detected, as recited by claim 5. Here, the Examiner refers to the CPU 1020 of Sokawa as allegedly corresponding to this feature of the claim. However, the specification does not appear to disclose that the CPU outputs a timing control signal corresponding to a detected frame rate. Instead, Sokawa makes the much more general disclosure of the CPU 1020 outputting a control signal. See col. 12, lines 25-26. Therefore, claim 5 is allowable for this additional reason.

Further, claim 11 is allowable over Sokawa for reasons analogous to those presented above for claim 5.

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

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The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,



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